CLAIMS:

1. Apparatus for controlling access to memory circuitry among a plurality of bus interfaces of a data processing system, comprising:

a plurality of ports respectively coupled to said plurality of bus interfaces; and

arbitration logic, in communication with said plurality of ports, for arbitrating access to said memory circuitry among said plurality of bus interfaces on a time-shared basis.

2. The apparatus of claim 1, further comprising:

a data bus and an address bus, each of said data bus and said address bus coupled to said plurality of ports;

data path logic configured to communicate signals between said data bus and said memory circuitry; and

address path logic configured to communicate signals between said address bus and said memory circuitry.

3. The apparatus of claim 2, further comprising:

a control bus coupled to said plurality of ports and said arbitration logic; and

control logic coupled to said arbitration logic and configured to couple signals to said memory circuitry.

4. The apparatus of claim 3, wherein each of said arbitration logic and said control logic is coupled to each of said data path logic and said address path logic.

5. The apparatus of claim 3, wherein said data path logic comprises:

a read interface having a pair of first-in-first-out (FIFO) memories for each of said plurality of ports;

a write interface having a pair of FIFO memories for each of said plurality of ports;

a multiplexer configured to select one pair of FIFO memories in said write interface; and

a first memory interface configured to communicate data between a data interface of said memory circuitry and each of said read interface and said selected pair of FIFO memories in said write interface; and

a second memory interface configured to communicate data between said selected pair of FIFO memories and a data mask interface of said memory circuitry.

6. The apparatus of claim 3, wherein said address path logic comprises:

a set of registers for each of said plurality of ports, each said set of registers configured to provide bank address data, row address data, and column address data;

a bank register, a row register, and a column register;

a first multiplexer configured to drive said bank, row, and column registers with bank, row, and column address data, respectively, of a selected one of said sets of registers;

bank control logic configured to drive a first address interface of said memory circuitry with bank address data stored in said bank register; and

address control logic configured to drive a second address interface of said memory circuitry with a selected one of row address data stored in said row register and column address data stored in said column register.

7. The apparatus of claim 3, wherein said control logic comprises:

a set of registers configured to receive a request for a memory transaction selected from a plurality of memory transactions;

an encoder, coupled to said set of registers, configured

to provide encoded data in response to said requested memory transaction;

a first read only memory (ROM) configured to store a sequence of sub-transactions for each of said plurality of memory transactions;

a second ROM configured to store a sequence of memory operations for each said sequence of sub-transactions stored in said first ROM, each of said memory operations comprising an n-bit word, where n is an integer;

selection logic configured to select a memory operation in a sequence of memory operations in a sequence of sub-transactions corresponding to said requested memory transaction in response to said encoded data; and

a register bank for storing an n-bit word of said selected memory operation and for driving a control interface and a data strobe interface of said memory circuitry in response to said stored n-bit word.

8. The apparatus of claim 3, wherein said control logic comprises:

an encoder configured to provide encoded data in response to a request for a memory transaction selected from a plurality of memory transactions;

a memory configured to store a sequence of sub-transactions for each of said plurality of transactions and a sequence of memory operations for each said sequence of sub-transactions, each of said memory operations comprising an n-bit word, where n is an integer; and

selection logic configured to select a memory operation in a sequence of memory operations in a sequence of sub-transactions corresponding to said requested memory transaction in response to said encoded data;

wherein said memory is further configured to drive a control interface and a data strobe interface of said memory circuitry in response to an n-bit word

of said selected memory operation.

9. The apparatus of claim 8, wherein said control logic is disposed within a programmable logic device, and wherein said memory of said control logic comprises a block random access memory (BRAM).

10. The apparatus of claim 1, wherein said memory circuitry comprises double data-rate (DDR) memory circuitry.

11. The apparatus of claim 10, wherein said memory circuitry comprises DDR synchronous dynamic random access memory (SDRAM).

12. The apparatus of claim 1, further comprising:

a direct memory access (DMA) controller for controlling access to said memory circuitry through at least one of said plurality of ports.

13. The apparatus of claim 1, wherein said plurality of bus interfaces comprises at least one processor bus interface.

14. The apparatus of claim 13, wherein said at least one processor bus interface comprises an instruction-side processor bus interface and a data-side processor bus interface.

15. The apparatus of claim 1, wherein said plurality of bus interfaces comprises at least one non-shared bus interface.

16. The apparatus of claim 15, wherein each said at least one non-shared bus interface comprises a streaming bus interface.

17. A method of controlling access to memory circuitry among a plurality of bus interfaces of a data processing system, comprising:

receiving a request for a memory transaction from one or more of said plurality of bus interfaces; and

arbitrating access to said memory circuitry among said plurality of bus interfaces on a time-shared basis to select a memory transaction request.

18. The method of claim 17, wherein said arbitrating step comprises:

assigning a time-slot to each of said plurality of bus interfaces;

within each said time-slot, assigning a priority to at least one of said plurality of bus interfaces; and

selecting a memory transaction request from one of said plurality of bus interfaces in response to said assigned time-slots and said assigned priorities.

19. The method of claim 18, further comprising:

reading or writing data from or to said memory circuitry in response to a data context of said selected memory transaction request; and

addressing said memory circuitry in response to an address context of said selected memory transaction request.

20. The method of claim 19, wherein said data is read from or written to said memory circuitry using a direct memory access (DMA) transfer.

21. The method of claim 19, further comprising:

coupling control signals to said memory circuitry in response to said selected memory transaction request.

22. The method of claim 18, further comprising:

storing a sequence of sub-transactions for each of a plurality of memory transactions;

storing a sequence of memory operations for each said sequence of sub-transactions;

performing each memory operation in a sequence of memory operations for each sub-transaction in a sequence sub-transactions corresponding to a memory transaction of said plurality of memory transactions selected in accordance with said selected memory transaction request.

23. The method of claim 17, wherein said step of receiving comprises:

obtaining a request for a memory transaction from a processor coupled to at least one of said plurality of bus interfaces.

24. The method of claim 17, wherein said plurality of bus interfaces comprises a non-shared bus interface, and wherein said step of receiving comprises:

obtaining a request for a memory transaction from said non-shared bus interface.

25. The method of claim 24, wherein said non-shared bus interface comprises a streaming bus interface.

26. A data processing system, comprising:

a system bus;

a processor coupled to said system bus;

a media access controller (MAC) having a first non-shared bus interface;

host interface logic having a second non-shared bus interface;

memory circuitry; and

a memory controller, comprising:

a set of ports including a first port coupled to said processor, a second port coupled to said system bus, a third port coupled to said MAC, and a fourth port coupled to said host interface logic; and

arbitration logic, in communication with said set of ports, for arbitrating access to said memory circuitry among said processor, said system bus, said MAC, and said host interface logic on a time-shared basis.

27. The system of claim 26, wherein said memory circuitry comprises double data-rate (DDR) memory circuitry.

28. The system of claim 26, wherein said memory controller further comprises:

a direct memory access (DMA) controller for controlling access to said memory circuitry through at least said third port and said fourth port.

29. The system of claim 26, wherein each said first non-shared bus interface and said second non-shared bus interface comprises a streaming bus interface.

30. The system of claim 26, wherein said memory controller is disposed within an integrated circuit.

31. The system of claim 30, wherein said integrated circuit comprises a programmable logic device, and wherein said memory controller is implemented using programmable logic of said programmable logic device.